DATA SHEET

74ALVCHT16835
18-bit registered driver (3-State)

Product data

2002 Jun 05

Philips
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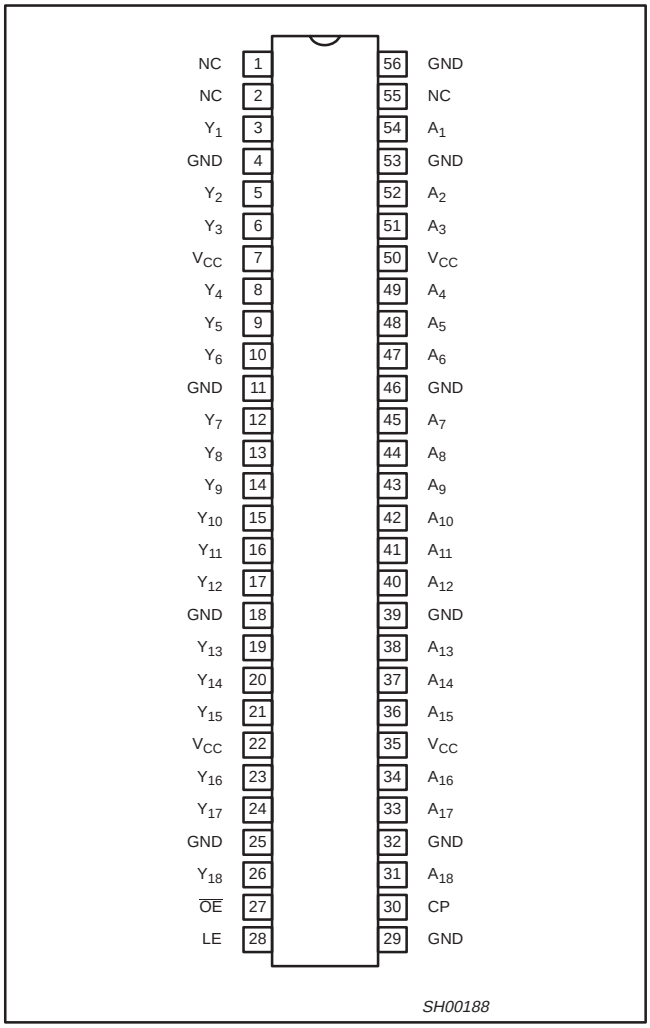
18-bit registered driver (3-State) 74ALVCHT16835

FEATURES

- Wide supply voltage range of 2.3 V to 3.6 V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Output drive capability 50 Ω transmission lines @ 85 °C
- ESD protection exceeds 1500 V HBM per JESD22-A114, A115 and 1000 V CDM per JESD22-C101
- Bus hold on data inputs eliminates the need for external pullup/pulldown resistors

PIN CONFIGURATION



DESCRIPTION

The 74ALVCHT16835 is a 18-bit registered driver. Data flow is controlled by active low output enable ($\overline{OE}$), active high latch enable (LE) and clock inputs (CP).

When LE is HIGH, the A to Y data flow is transparent. When LE is LOW and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip-flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay An to Yn; LE to Yn; CP to Yn	V_{CC} = 3.3 V, C_L = 50 pF		2.3 2.7 2.2	ns
f_{max}	Maximum clock frequency	V_{CC} = 3.3 V, C_L = 50 pF		350	MHz
C_I	Input capacitance			4.0	pF
$C_{I/O}$	Input/Output capacitance			8.0	pF
C_{PD}	Power dissipation capacitance per buffer	V_I = GND to V_{CC}[1]	transparent mode Output enabled Output disabled	13 3	pF
			Clocked mode Output enabled Output disabled	22 15	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacitance in pF; f_o = output frequency in MHz; V_{CC} = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

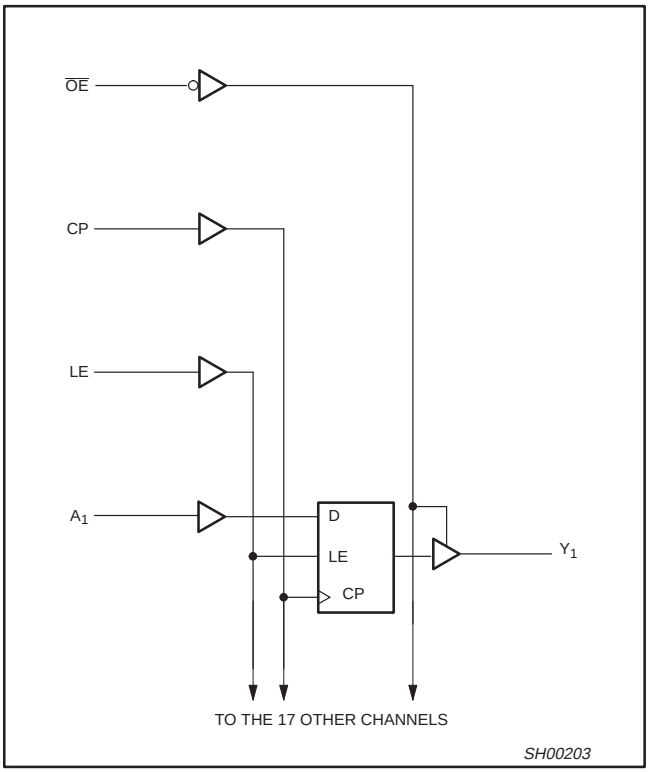
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
56-Pin Plastic TSSOP (TVSOP), 0.4 mm pitch	–40 to +85 °C	74ALVCHT16835DGV	SOT481-2

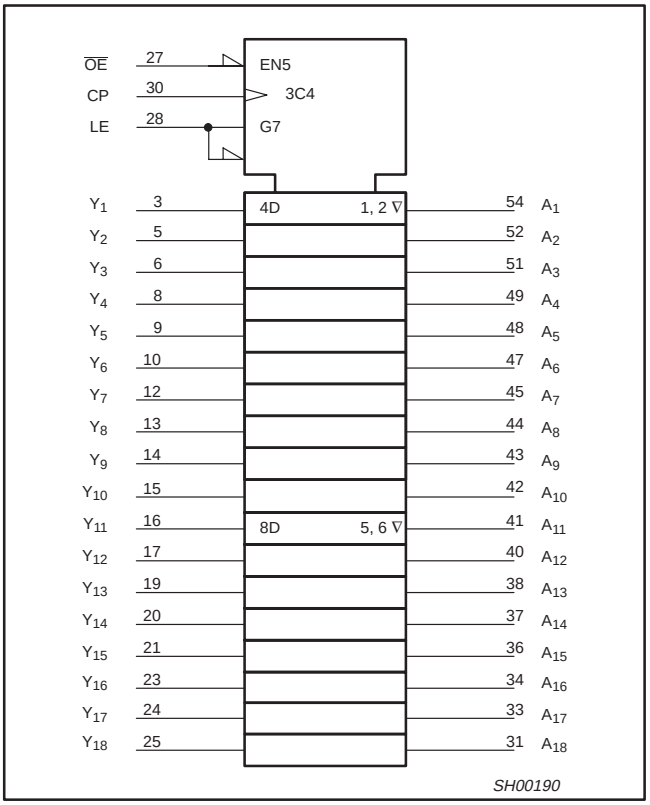
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 55	NC	No connection
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	Y_1 to Y_{18}	Data outputs
4, 11, 18, 25, 29, 32, 39, 46, 53, 56	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage
27	$\overline{OE}$	Output enable input (active LOW)
28	LE	Latch enable input
30	CP	Clock input
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	A_1 to A_{18}	Data inputs

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{OE}$	LE	CP	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0[1]
L	L	L	X	Y_0[2]

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

NOTES:
1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
2. Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC supply voltage 2.5 V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3 V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
	DC supply voltage (for low-voltage applications)		2.3	3.6	
V_I	DC Input voltage range		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0 V V_{CC} = 3.0 to 3.6 V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +4.6	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	± 50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	± 50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		± 100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package -plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 8 mW/K	600	mW
Θ_{JA}	Package thermal impedance	See Note 2	93	°C/W

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = –40 to +85 °C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 2.3 to 2.7 V	1.7	1.2	—	V
		V_{CC} = 2.7 to 3.6 V	2.0	1.5	—	
V_{IL}	LOW level Input voltage	V_{CC} = 2.3 to 2.7 V	—	1.2	0.7	V
		V_{CC} = 2.7 to 3.6 V	—	1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.3 to 3.6 V; $V_I = V_{IH}$ or V_{IL}; I_O = –100 µA	V_{CC} – 0.2	V_{CC}	—	V
		V_{CC} = 2.3 V; $V_I = V_{IH}$ or V_{IL}; I_O = –6 mA	V_{CC} – 0.3	V_{CC} – 0.08	—	
		V_{CC} = 2.3 V; $V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	V_{CC} – 0.6	V_{CC} – 0.26	—	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	V_{CC} – 0.5	V_{CC} – 0.14	—	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = –12 mA	V_{CC} – 0.6	V_{CC} – 0.09	—	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = –24 mA	V_{CC} – 1.0	V_{CC} – 0.28	—	
V_{OL}	LOW level output voltage	V_{CC} = 2.3 to 3.6 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100 µA	—	GND	0.20	V
		V_{CC} = 2.3 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6 mA	—	0.07	0.40	V
		V_{CC} = 2.3 V; $V_I = V_{IH}$ or V_{IL}; I_O = 12 mA	—	0.15	0.70	V
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 12 mA	—	0.14	0.40	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 24 mA	—	0.27	0.55	
$I_{I(hold)}$		V_{CC} = 2.3 V; V_I = 0.7 V	45	—	—	µA
		V_{CC} = 2.3 V; V_I = 1.7 V	–45	—	—	
		V_{CC} = 3.0 V; V_I = 0.8 V	75	—	—	
		V_{CC} = 3.0 V; V_I = 2.0 V	–75	—	—	
		V_{CC} = 3.6 V; V_I = 0 to 3.6 V	—	—	±500	
I_I	Input leakage current	V_{CC} = 2.3 to 3.6 V; $V_I = V_{CC}$ or GND	—	0.1	5	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 2.3 to 3.6 V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND	—	0.1	10	µA
I_{CC}	Quiescent supply current	V_{CC} = 2.3 to 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0	—	30	60	µA
ΔI_{CC}	Additional quiescent supply current	V_{CC} = 2.3 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0	—	150	400	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND V_{CC} = 3.3 V	—	3.5	—	pF
	Data inputs		—	6	—	
C_o	Outputs	$V_O = V_{CC}$ or GND V_{CC} = 3.3 V	—	7	—	pF

NOTE:

1. All typical values are at T_{amb} = 25 °C.

AC CHARACTERISTICS FOR V_{CC} = 2.3 V TO 2.7 V RANGE

GND = 0 V; $t_r = t_f \leq 2.0$ ns; C_L = 30 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 2.3 to 2.7 V			
			MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 7	1.3	3.0	4.7	ns
	Propagation delay LE to Yn	2, 7	1.4	3.6	5.7	
	Propagation delay CP to Yn	4, 7	1.2	3.0	4.7	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	6, 7	1.4	3.7	5.3	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	6, 7	1.0	2.5	3.7	ns
t_W	CP pulse width HIGH or LOW	4, 7	3.3	—	—	ns
	LE pulse width HIGH	2, 7	3.3	—	—	
t_{SU}	Set-up time An to CP	5, 7	0.1	—	—	ns
	Set-up time An to LE	3, 7	0.7	—	—	
t_h	Hold time An to CP	5, 7	0.4	—	—	ns
	Hold time An to LE	3, 7	0.1	—	—	
t_{sk}	Output skew		—	—	0.5	ns
f_{max}	Maximum clock pulse frequency	4, 7	150	—	—	MHz

NOTE:
1. All typical values are at V_{CC} = 2.5 V and T_{amb} = 25 °C.
2. Output skew is not production tested

AC CHARACTERISTICS FOR V_{CC} = 3.0 V TO 3.6 V RANGE AND V_{CC} = 2.7 V

GND = 0 V; $t_r = t_f \leq 2.5$ ns; C_L = 50 pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS			LIMITS			UNIT
			$V_{CC} = 3.3 \pm 0.3$ V			V_{CC} = 2.7 V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PHL}/t_{PLH}	Propagation delay An to Yn	1, 7	1.2	2.3	3.6	1.3	2.7	3.8	ns
	Propagation delay LE to Yn	2, 7	1.3	2.7	4.2	1.4	3.0	4.9	
	Propagation delay CP to Yn	4, 7	1.0	2.2	3.7	1.2	2.3	3.7	
t_{PZH}/t_{PZL}	3-State output enable time $\overline{OE}$ to Yn	6, 7	1.0	2.3	3.8	1.4	2.4	4.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $\overline{OE}$ to Yn	6, 7	1.0	2.5	3.7	1.0	2.5	3.7	ns
t_W	CP pulse width HIGH or LOW	4, 7	2.0	—	—	2.0	—	—	ns
	LE pulse width HIGH	2, 7	2.0	—	—	2.0	—	—	
t_{SU}	Set-up time An to CP	5, 7	0.1	—	—	0	—	—	ns
	Set-up time An to LE	3, 7	0.5	—	—	0	—	—	
t_h	Hold time An to CP	5, 7	0.4	—	—	0.5	0.3	—	ns
	Hold time An to LE	3, 7	0.1	—	—	0.25	0.4	—	
t_{sk}	Output skew[3]		—	—	—	—	—	0.5	ns
f_{max}	Maximum clock pulse frequency	4, 7	150	—	—	150	—	—	MHz

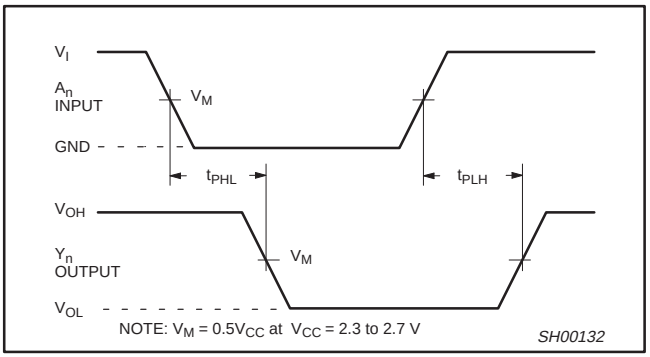
NOTES:
1. All typical values are measured T_{amb} = 25 °C.
2. Typical value is measured at V_{CC} = 3.3 V
3. Output skew is not production tested

AC WAVEFORMS FOR V_{CC} = 3.0 V TO 3.6 V AND V_{CC} = 2.7 V RANGE

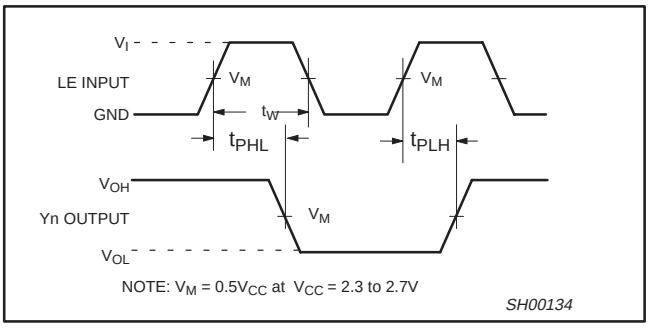
V_M = 1.5 V
$V_X = V_{OL}$ + 0.3 V
$V_Y = V_{OH}$ – 0.3 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
V_I = 2.7 V

AC WAVEFORMS FOR V_{CC} = 2.3 V TO 2.7 V AND V_{CC} < 2.3 V RANGE

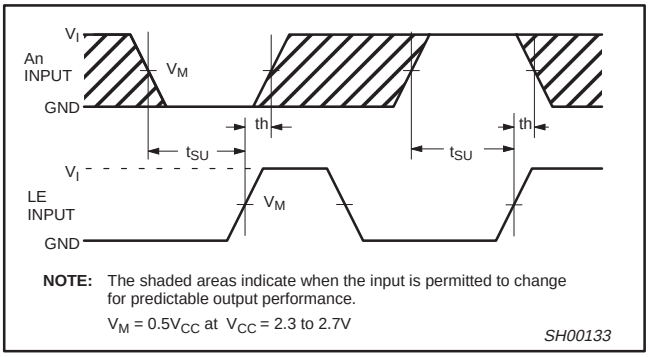
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL}$ + 0.15 V
$V_Y = V_{OH}$ – 0.15 V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$



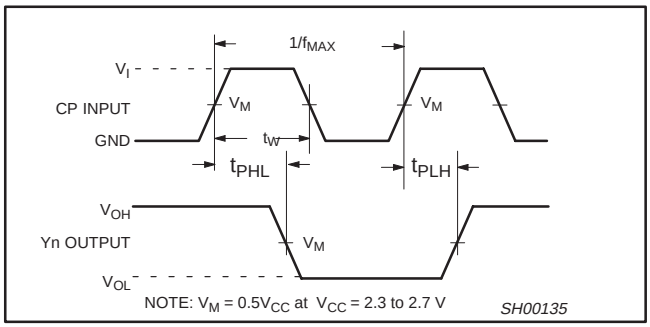
Waveform 1. Input (An) to output (Yn) propagation delay



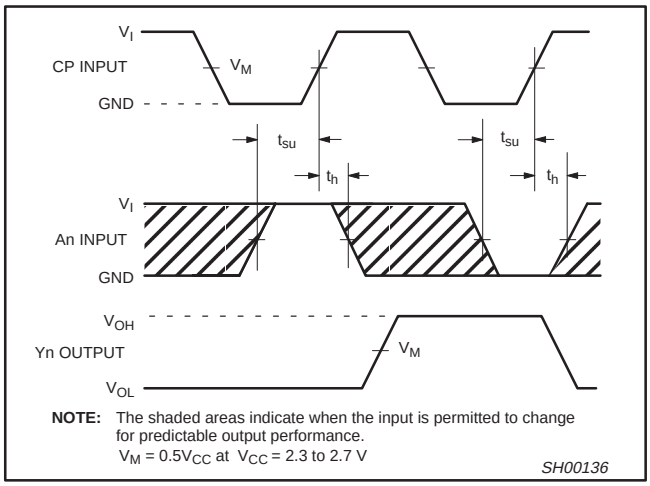
Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.



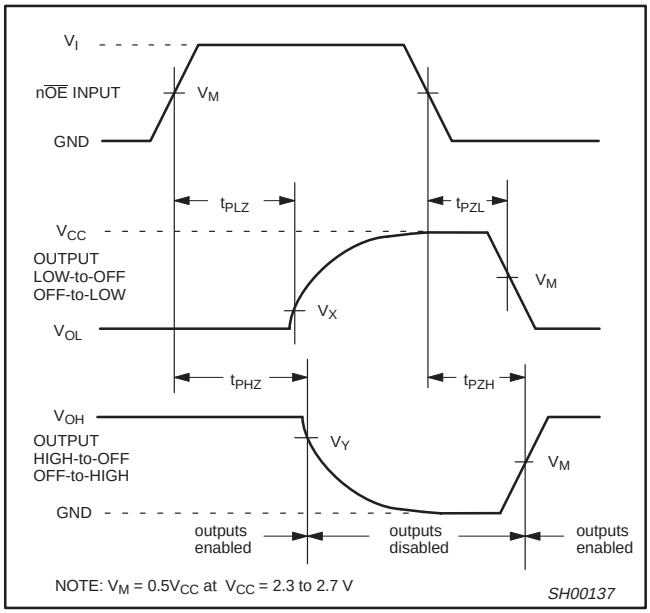
Waveform 3. Data set-up and hold times for the An input to the LE input



Waveform 4. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.

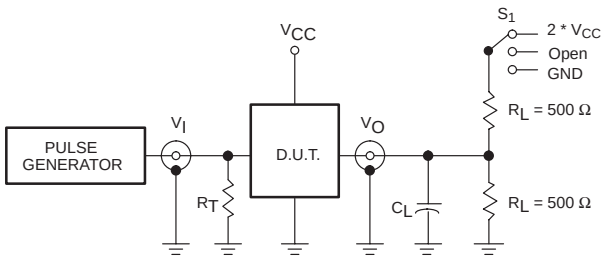


Waveform 5. Data set-up and hold times for the An input to the clock CP input



Waveform 6. 3-State enable and disable times

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SWITCH POSITION

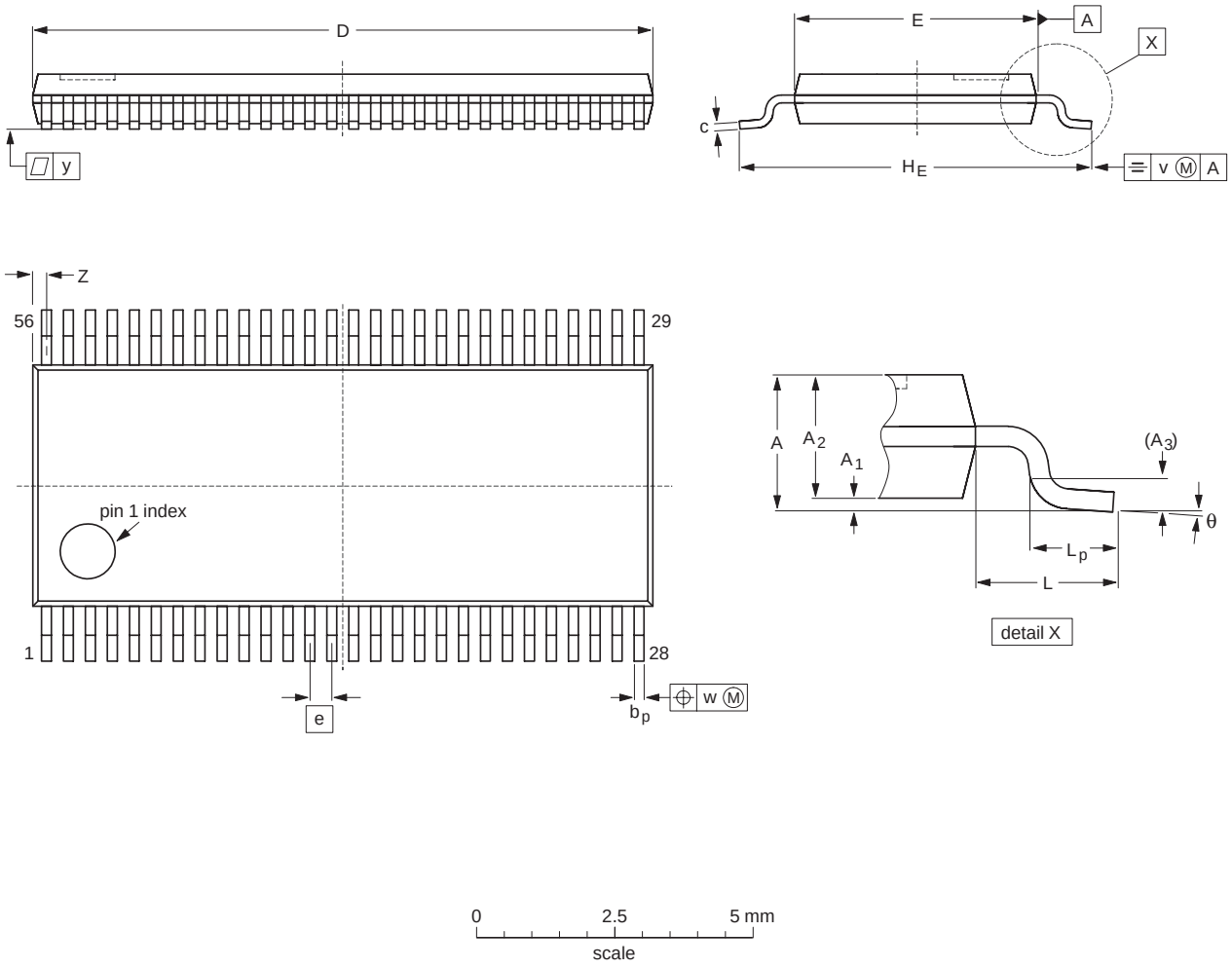
TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_I
< 2.7V	V_{CC}
2.7–3.6V	2.7V

SV00906

Waveform 7. Load circuitry for switching times

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 4.4 mm **SOT481–2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A1	A2	A3	bp	c	D (1)	E (2)	e	HE	L	Lp	v	w	y	Z (1)	θ
mm	1.2	0.15 0.05	1.05 0.80	0.25	0.23 0.13	0.20 0.09	11.4 11.2	4.5 4.3	0.4	6.6 6.2	1	0.75 0.45	0.2	0.07	0.08	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT481–2	– – –	MO–194	– – –			01–11–24

NOTES

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Date of release: 06-02

Document order number: 9397 750 09943

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